17. (amended) A semiconductor processing unit according to claim 10, further comprising:

an alignment chamber having [an] the alignment means, [a] the buffer means and a first conveying means,

a containing means arranged adjacently to the alignment chamber, for containing [a plurality of substrates] the substrate,

a load-lock means arranged adjacently to the alignment chamber,

a conveying chamber arranged adjacently to the load-lock means, having a second conveying means, and

a vacuum processing chamber arranged adjacently to the conveying chamber, for conducting a vacuum process to [a] the substrate,

wherein the first conveying means is adapted to take out [a] the substrate from the containing means, to pass the substrate to the buffer means, to receive the substrate from the stage of the alignment means and to convey the substrate to the load-lock means, and

the second conveying means is adapted to receive the substrate from the load-lock means and convey the substrate to the vacuum process chamber.

17. A semiconductor processing unit according to claim 10, further comprising:

an alignment chamber having the alignment means, the buffer means and a first conveying means,

a containing means arranged adjacently to the alignment chamber, for containing the substrate,

a load-lock means arranged adjacently to the alignment chamber,

a conveying chamber arranged adjacently to the load-lock means, having a second conveying means, and

a vacuum processing chamber arranged adjacently to the conveying chamber, for conducting a vacuum process to the substrate,

wherein the first conveying means is adapted to take out the substrate from the containing means, to pass the substrate to the buffer means, to receive the substrate from the stage of the alignment means and to convey the substrate to the load-lock means, and

the second conveying means is adapted to receive the substrate from the load-lock means and convey the substrate to the vacuum process chamber.